Abstract of the Disclosure

An address buffer in a semiconductor memory device includes a differential input unit receiving a reference voltage and an address signal, a current mirroring unit connected between the differential input unit and a first voltage, a biasing unit, which is connected between the differential input unit and a second voltage, for supplying bias current to the differential input unit and the current mirroring unit, and a controlling unit for enabling/disabling the biasing unit by receiving a refresh signal and a bank active signal.